Kathmandu University
Department of Electrical and Electronics Engineering
ELECTRONICS AND ANALOG FILTER DESIGN LAB

EXPERIMENT 11: BJT Inverter and DTL Logic

Objectives: To Plot the VTC of a BJT Inverter in Oscilloscope
Verification of Truth Table of Modified DTL NAND Gate

Materials and Equipment:
82nF [1] 1K [2] 2N222A [1] Diode [3] Bread Board [1] Probes [3] Function Generator

Theory
The operating point for a BJT inverter as shown in fig 1 is defined by the point of intersection of load line with the output characteristics of the transistor.

For a small magnitude of base current the transistor is in cut-off condition. For a large magnitude of base current the transistor saturates and works as a linear amplifier in the region between cut-off and saturation. To take the transistor out of saturation quickly, reverse base current is required in order to remove the excess stored base charge.

When an inverter as shown in fig 2 is driving a capacitive load it takes certain time for the transistor to go from saturation to cut-off determined by RC_L time constant, where R is the collector load. If we use low value of R (capacitor charged by large current), RC_L time constant reduces but a large collector current is required to saturate the transistor. For the case when transistor goes from cut-off to saturation we require a large R (in order to reduce the collector current). This conflicting requirement is meet in the TTL gates by using active pull up.

In the basic DTL NAND gate as shown in fig 3, the transistor never goes into cut-off (Since the transistor is forward biased by the low state input voltage (v_{IL}) and the drop across the diode). The modified DTL gate in fig 4 removes this problem by using additional diode.

Procedure

Without Capacitive Loading

1. Connect the circuit as shown in fig 1
2. Don't forget to give (0-5) V triangular wave with 2.5V DC offset
3. See in dual mode the input and output waveform
4. Note the approximate voltage at the input when the inverter changes its state

V_{In}	V_{OUT}
<	

V_{In}	V_{OUT}
>	

5. Plot the VTC of the inverter using XY mode of the oscilloscope
6. From the VTC complete table 1.

Table 1

V_{IN}	V_{OUT}

Table 2

V_B	V_{OUT}

7. Taking the input from base of transistor complete table 2
8. Remove CHX and see CHY only (Output of inverter) in YT mode
9. Set scope in X10 magnification
10. Note the rise time and fall time of the pulse waveform. *Remember 10% to 90%*

Rise Time (t_r)	Fall Time (t_f)

With Capacitive Loading

11. Connect 82nF capacitor across collector resistor
12. Note the charging time and discharging time
13. Sketch the waveform

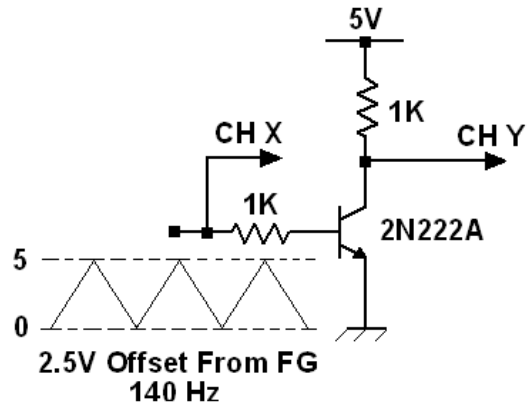

Fig: - 1

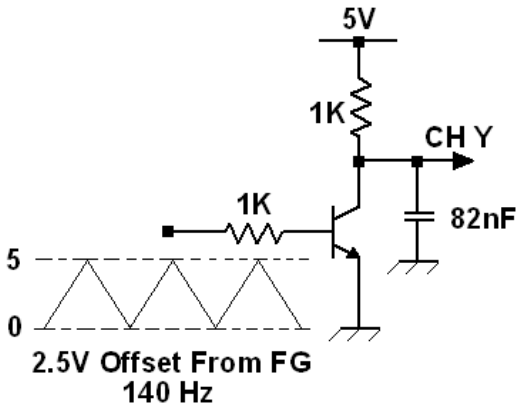

Fig: - 2

Basic DTL NAND Gate

1. Turn OFF the function generator
2. Connect the circuit as shown in fig 3
3. Complete table 3

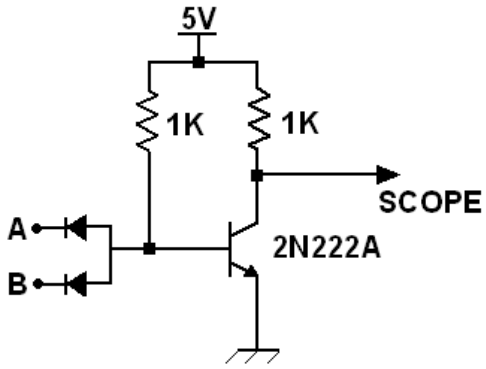

Fig: - 3

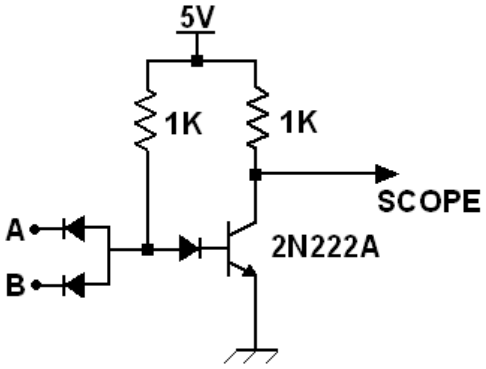

Fig: - 4

Modified DTL NAND Gate

4. Connect the circuit as shown in fig 4
5. Complete table 4

Table 3

A	B	Y
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Table 4

A	B	Y
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Conclusion

In DTL gate of fig 4, there is no path for reverse base current. This problem is solved in TTL gate by using multi emitter transistor.