Kathmandu University
Department of Electrical and Electronics Engineering
ELECTRONICS AND ANALOG FILTER DESIGN LAB

EXPERIMENT 9: Phase Locked Loop

Objectives: To Understand the Concept of Lock Range and Capture Range in a PLL

To Plot the Input Frequency and Control Voltage of VCO Characteristics within the Lock Range

Materials and Equipment:
0.001uF [2] 10uF [1] 12K [1] IC 565 [1] Probe [3] Bread Board [1] Multimeter [1]

Theory:
Phase Locked Loop (PLL) is basically the application of negative feedback with unity feedback factor and acts as a phase follower. The block diagram of a second order PLL is given in fig 1.1

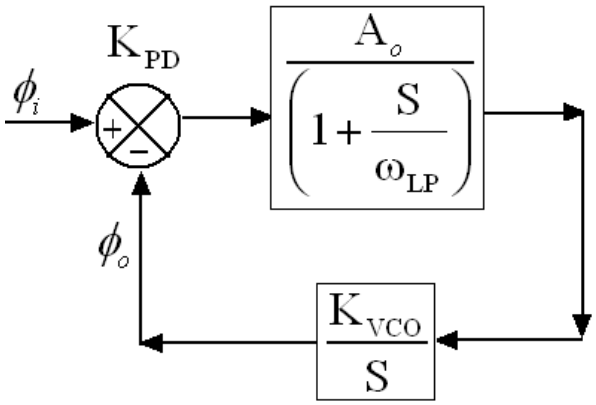


Fig 1.1

ϕ_i and ϕ_o are the input phase and output phase. A_o is the DC gain of the amplifier. ω_{LP} is the LPF cut-off frequency. K_{PD} and K_{VCO} are the sensitivity of phase detector and VCO respectively. The transfer function of second order PLL is given by

$$\frac{\phi_o}{\phi_i} = \frac{1}{1+\frac{S}{K_l}+\frac{S^2}{K_l \omega_{LP}}}$$

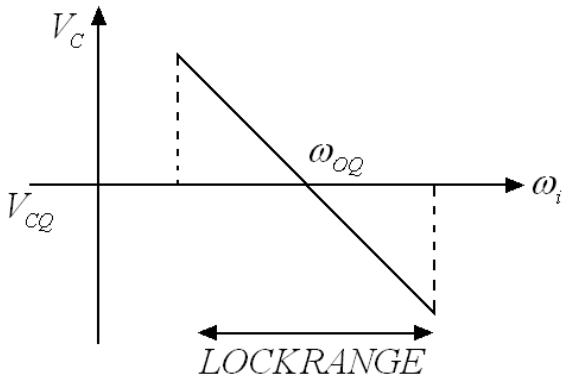
K_l is the DC loop gain and is equal to the product of K_{PD}, K_{VCO} and A_o.

When there is no input frequency then VCO will continue to run in its own free running state. The free running frequency is determined by external resistor and capacitor.
When the input frequency to the phase detector is equal to the free running frequency of PLL then input frequency and output frequency will be out of phase by 90^o.
When the input frequency slowly varies around the free running frequency of PLL then PLL will track the change in input frequency up to the *LOCK Range.* The lock range is given by πK_l.

Capture Range is the frequency range over which the maximum likelihood of detection of the incoming frequency is high. It depends upon the lock range and LPF cut-off frequency. The capture range of PLL is given by

$$\Delta\omega_C = \pm\sqrt{\frac{\pi}{2} K_l \omega_{LP}}$$

Characteristics of ω_i and control Voltage of VCO (V_C) within the Lock Range



This shows when $\omega_i = \omega_{OQ}$ then $V_C = V_{CQ}$. When $\omega_i > \omega_{OQ}$ then $V_C < V_{CQ}$. When $\omega_i < \omega_{OQ}$ then $V_C > V_{CQ}$. These all are only valid within the lock range.

IC 565

It is a PLL IC with operating frequency range from 0.001Hz to 500 kHz. Other characteristics are given below.

Operating voltage range: ±6V to ±12V
Minimum input level required for tracking: 10 mV rms

Free running frequency: $f_{OUT} \cong \frac{1.2}{4R_1C_1} Hz$

Lock Range: $f_L = \pm\frac{8 f_{OUT}}{V} Hz$ V= (+V) – (-V) (Volts)

Capture Range: $f_C = \pm\left[\frac{f_L}{(2\pi)(3.6)(10^3)(C_2)}\right]^{\frac{1}{2}}$

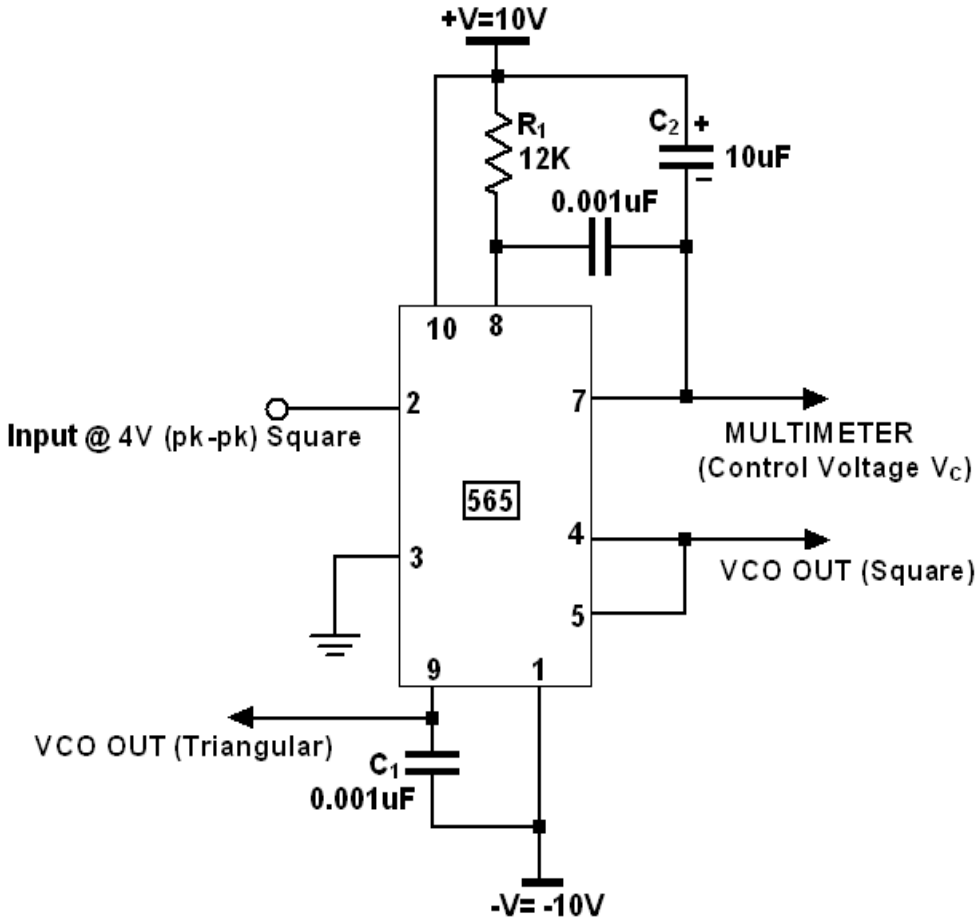


Fig 1.2: - Pin configuration of 565 PLL IC

Procedure

1. First theoretically calculate the free running frequency of PLL, lock range and capture range. *[Answer: 25kHz, ± 10kHz, ± 210Hz]*
2. Without giving any input to the PLL measure the free running frequency of PLL through PIN 4.
3. Measure the output through PIN9 and compare the frequency of square wave and triangular wave.
4. Note the amplitude of both triangular wave and square wave.
5. Set the function generator at 4V (pk-pk) square wave @ free running frequency and give it to PIN2.
6. Note the phase difference between input and output frequency.
7. Note the multimeter reading through PIN7.

Input Frequency and Control Voltage Characteristics

ω_i (kHz)	V_C (Volts)	ω_i (kHz)	V_C (Volts)
25		24	
26		23	
27		22	
28		21	
29		20	
30		19	
31		18	
32		17	
33		16	
34		15	
35		14	
36		13	
37		12	
38		11	

8. Constantly monitor the output through PIN4 when you change the input frequency through PIN2. [See PIN2 and PIN4 output in Dual Mode]
9. Note how phase changes between input and output frequency when the input frequency varies within the lock range.
10. Determine the Lock Range and Capture Range.