Experiment __: Design of 4 bit BCD adder using 4 bit binary adder(IC 4008) and primitive gates.

Theory:

BCD Adder:

- Each input to the BCD adder doesn't exceed 9, the sum cannot be greater than (9+9+1=19), and the 1 in the sum being input carry.
- The 4 bit binary adder gives output sum in binary and produce a result ranges from 0 through 19.

- Follows the rules of binary addition to give the Sum and Carry outputs after adding two bits

Truth Table:

Binary Sum					BCD Sum					Decimal
K	Z8	Z4	Z2	Z1	C	S8	S4	S2	S1	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

From truth table it is apparent that when binary sum is less than 1001, the corresponding BCD number is identical, so no conversion is required.

When binary sum is greater than 1001, we obtain non valid BCD representation. The addition of 6 (0110) to the binary sum converts it to the correct BCD representation and also produces an output carry as required.

- The block diagram including logic circuit with necessary correction for BCD addition is shown below.
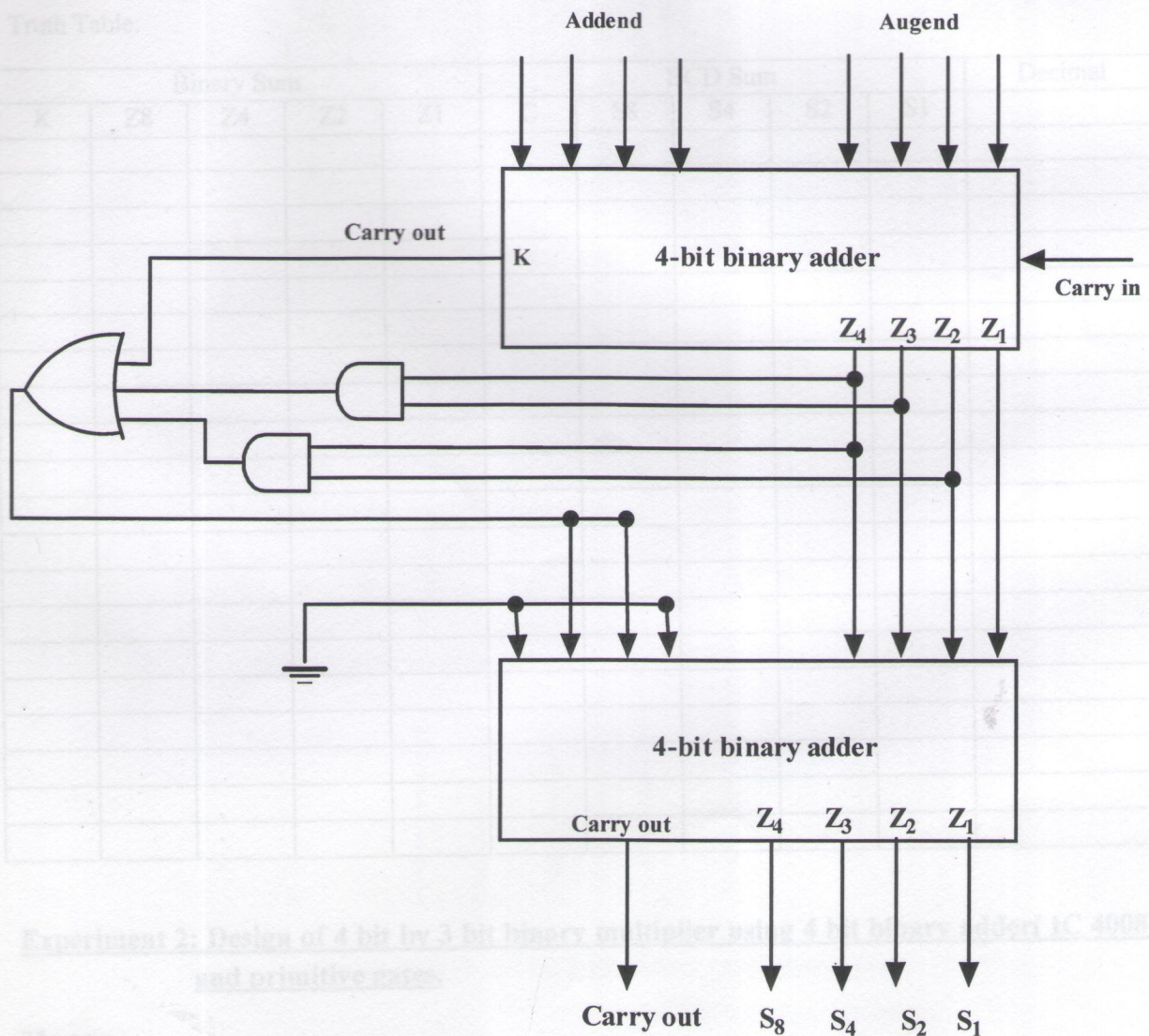

Figure1: BCD adder circuit

Procedure:

- Connect the above circuit in the multisim.
- For logic 1, connect to Vcc and for logic 0, connect to ground.

- For truth table verification use SPST switches.
- To observe output use virtual lamp or virtual LEDS.
- Tabulate the truth table of BCD adder.

Observation Table:

Truth Table:

Binary Sum					BCD Sum					Decimal
K	Z8	Z4	Z2	Z1	C	S8	S4	S2	S1	

Experiment 2: Design of 4 bit by 3 bit binary multiplier using 4 bit binary adder(IC 4008) and primitive gates.
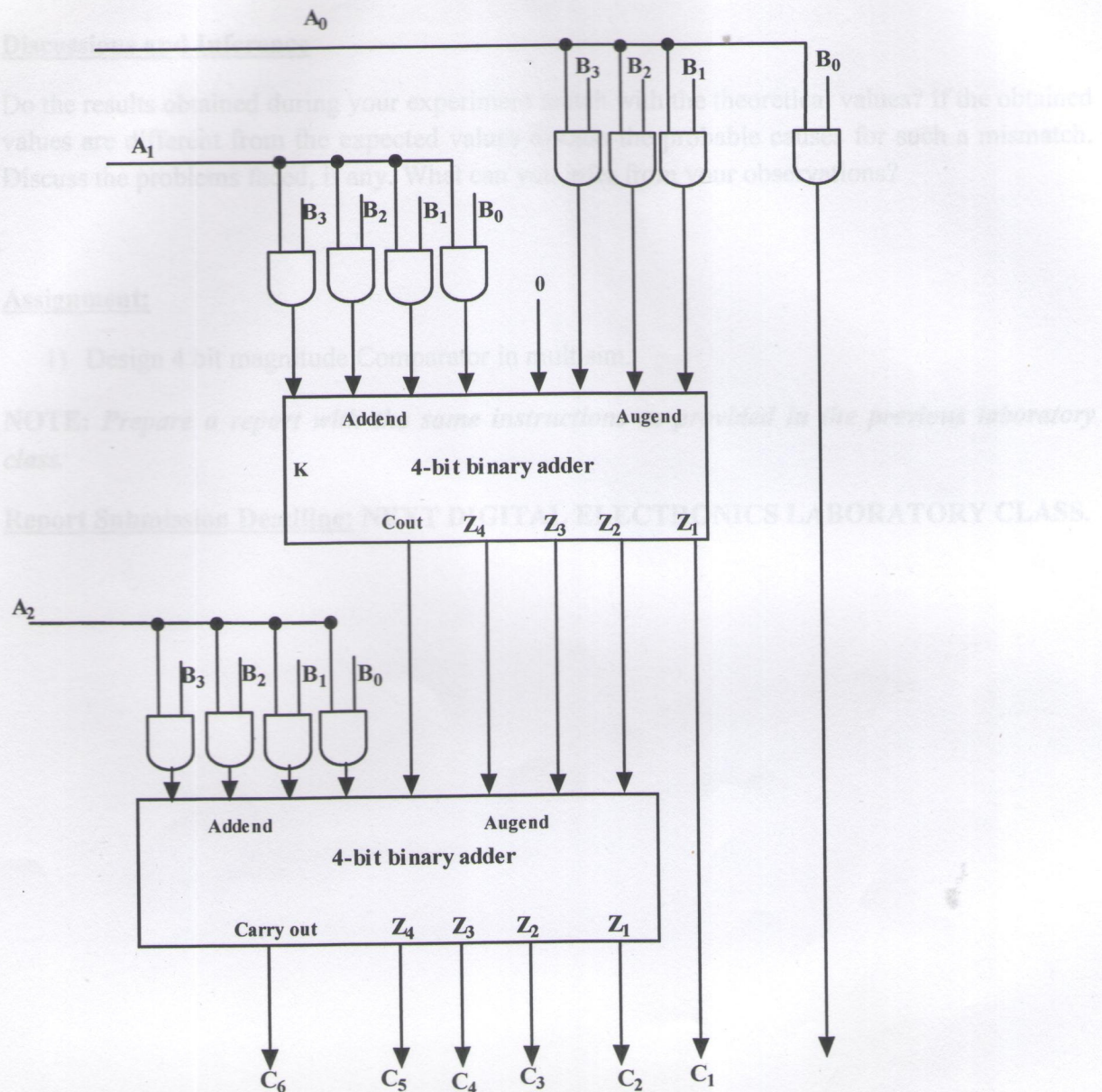
Theory:

Binary Multiplier

- Multiplicand is multiplied by each bit of the multiplier starting from the least significant bits.
- Successive partial products are shifted one position to the left.
- Final product is obtained from the sum of the partial products.

The block diagram of the 4- bit by 3-bit binary multiplier is shown below:

Figure 4: 4- bit by 3-bit binary multiplier

Procedure:

- Connect the above circuit in the multisim.
- For logic 1, connect to Vcc and for logic 0, connect to ground.
- For truth table verification use SPST switches.
- To observe output use virtual lamp or virtual LEDS.
- Tabulate the truth table of BCD adder.