Course Title: Digital Circuit and System Design
Course Code: EEEG 320
Credit Hours: 3

Course Description:
To provide an understanding of modern techniques used in the design and analysis of very large scale digital circuits

Course Contents:

Unit 1: Review of Digital Logic and Electronics Engineering
Logic gates, boolean algebra, simplification of switching functions, combinational logic, sequential logic, DTL, RTL, TTL, BJT, FET, CMOS.

Unit 2: Digital Circuits
Scale of integration, logic families, logic levels, noise margins, fan-out and fan-in, delay, power, area, CMOS logic, latches and flip-flops, clock cycle and timing paths, tristate

Unit 3: Very High Speed Integrated Circuit Hardware Description Language
Overview of Hardware Description Language, Basic Very High Speed Integrated Circuit Hardware Description Language (VHDL) Concept, Structural Description and Behavioral Description, Test-bench, Skeleton of a Basic VHDL Program, Entity Declaration and Architecture Body, Design Unit and Library, Sequential Statements of VHDL, VHDL Process, and IF, CASE, FOR loop Statement

Unit 4: Memory Devices
Terminologies, general memory operation, ROMs and RAMs, power-down storage, cache memory, FIFO.

Unit 5: Asynchronous Sequential Circuits
Types, analysis and synthesis of pulse-mode circuits, analysis and synthesis of fundamental-mode circuits, races, cycles hazards.

Unit 6: Design Implementation
Custom ICs, ASICs, programmable devices.

Unit 7: Combinational Circuit Design with Programmable Logic Devices
Logic array circuits, field-programmable, realizing logic functions with PROMs, LUT, programmable array logic.

Unit 8: Sequential Circuit Design with Programmable Logic Devices
Registered programmable logic devices, programmable gate arrays

Unit 9: Optimization of Logic
Improving timing, area and power, partitioning.

Unit 10: Logic Circuit Testing and Testable Design
Fault models, combinational logic circuit testing, sequential logic circuit testing, design for testability, BIST.

Unit 11: Field Programmable Gate Arrays Prototyping
Introduction to Field Programmable Gate Arrays (FPGA), Overview of the Xilinx Spartan-3 devices, Development Flow, Overview of the Xilinx ISE Project Navigator , Synthesis and Physical Design, Verification and Testing

References:
1. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, Pearson Education
2. R. J. Tocci, *Digital Systems*, Prentice-Hall
3. V. P. Nelson, H. T. Nagle, J. D. Irwin, and B. D. Carrol, *Digital Logic Circuit Analysis & Design*, Prentice-Hall
4. Pong P. Chu, " *RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability*", Wiley, Latest Edition

Evaluation:
In-Semester Evaluation: 50%
End-Semester Evaluation: 50%