Course Title: Very Large Scale Integrated Circuits
Course Code: ETEG 426
Credit Hours: 3

Course Description:
This course covers the design principles of VLSI circuits. Issues of low level circuit and layout design are investigated with the aid of CAD tools. Higher-level design issues are addressed via theoretical models that facilitate cost analyses.

Course Contents:

Unit 1: Introduction
VLSI Technology trends, Moore's law

Unit 2: Difference between MOS and BJTs
MOS transistor characteristics, Types of MOS transistors; NMOS and CMOS inverter circuits and transmission gates, Inverter circuit operation, Rationed logic; Structure of NMOS and CMOS inverter

Unit 3: NMOS and CMOS Circuits for Combinational and Sequential logic
Stick notation, Shannon's expansion theorem and realization of Boolean functions, PLA generators, Pseudo NMOS circuits, Clocked logic, Simple flip flop realization using NMOS and CMOS, Shift register, Dynamic shift registers, Superbuffers, RAM and ROMS

Unit 4 : VLSI Fabrication Techniques
Lithographic process ; Twin-tub and SOS process ; Design rules, Specification of layers

Unit 5: Delay and Timing Calculation
Power estimates

Unit 6: System Design
VLSI Design levels, System design examples

Unit 7: CAD tools for VLSI
Design steps; CIF representation, Design styles, Placement, routing, Simulation, Circuit extraction, Design rules, Checking algorithms; Hardware description languages; Testability fault tolerance; Introduction to silicon compilers.

References:
1. D. A .Pucknell and K. Eshrangian, *Basic VLSI Design Systems and circuits*, PHI
2. Eugene D. Fabricius, *Introduction to VLSI design*
3. Mead and Conway, *Introduction to VLSI systems*, Addison Wesley
4. Amar Mukherjee, *Introduction to NMOS and CMOS VLSI system design*, PHI

Evaluation:
In-Semester Evaluation: 50%
End-Semester Evaluation: 50%